Class 1: Introduction to Very Large Scale Integrated Circuits

Course # : 0512-4703

Prerequisites: Digital Logic systems; Electronic Devices.

Sylabus: Introduction: CMOS gates, memories, analog and mixed signal circuits, examples. MOS transistor review: models, static gates, transmission gates, tristate, BiCMOS. CAD tools: layout (LEDIT) and circuit (SPICE). CMOS process reviewer, design rules. Preliminary design: parameter evaluation, rise and fall time estimation, sizing, power estimation, design margining, reliability and scaling. CMOS circuit design: logic selection, timing, IO circuits, lower power design. Design strategies and options: standard cell, gate array, PLD, symbolic design, design verification, data path, examples. Chip design – examples for DSP, memories and processors.

Goals

1. The student should be capable to design building blocks of digital integrated VLSI circuits.
2. The student should know to simulate small to medium level VLSI circuits and systems.
3. The student should know to verify small to medium digital circuits including data path and memories.
4. The student should know to quickly estimate the performance of large VLSI circuits, using manual calculations
5.. The student should be able to work in team designing very large scale integrated circuits.

Curriculum (Course # : 0512-4703, continue)

Week		
1	Introduction	Historical notes, scaling laws, Issues in digital design, design metrics
2	Design rules and the CMOS process	CMOS process overview, front end, backend, Design rules, packaging
3	The devices	Present intuitive understanding of device Operation, Introduction of basic device equations, Introduction of models for manual analysis, Introduction of models for SPICE Simulation, Analysis of secondary and deep-sub-micron effects, Future trends
4	The wire	Interconnects, modeling, delay times, parasitic components: resistance, capacitance, inductance. Elmore's rule.
5	The Inverter	CMOS Inverter, Voltage Transfer Characteristic, corners, propagation delay, inverter sizing, power dissipation, Impact of Technology Scaling
6-7	Designing Combinational Logic Circuits	Combinational vs. Sequential Logic, Static CMOS Circuit, dynamic SMOC circuits, standard cells, transistor sizing, fan-in, fan-out, logical effort, Delay in a Logic Gate, Optimum Effort per Stage, Ratioed Logic, Pass-Transistor Logic, Dynamic Logic
8-9	Design Methodologies	System on a chip, data path, Implementation Choices, gate arrays, FPGA
10-11	Coping with Interconnect	Interconnect modeling part 2, cross talk, ESD, drivers, reliability, electromigration,
12-13	Memories	Memory Classification, Memory Architectures, The Memory Core, Periphery, reliability, case studies